The Design and Performance of SpaceWire Router-network using CSP

Session:Components

Short Paper

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Abstract

We have designed an IEEE1355 network router as an Intellectual Property (IP) core. The basic idea of the router design has been evaluated, refined and verified from the point of view of robustness and security using CSP (Communication Sequential Processes) method, one of formal design methods [1]. Functionality of the router has been confirmed by implementing it in a network formed with several TPCOREs. TPCORE[2] is our homemade processor that can execute the same instruction set as transputer. Since all the network components have been implemented in a single FPGA chip, we realized Network on Chip (NoC). In this report we discuss the functionality of the router, modification of a TPCORE for IEEE1355 and performance of the network.

1 TPCORE

TPCORE has been developed by the authors' group a few years ago to make a simple parallel network system without introducing any operating system. We have known that we implemented such a system if we could use a transputer, which has been developed by an English company called Inmos Limited in 1980s and used worldwide extensively in that days. Since a parallel processing language occam[1] is closely related to the transputer architecture, programs written in occam were only able to run in a transputer or a transputer network. A transputer has

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[1]Occam has been originally developed by Inmos Limited inspired by CSP[3]. Re-

four external serial link interfaces. This interface is called as os-link conveniently[2]. Connecting an os-link port with one of another transputer, we can form a network with several transputers in a plug-and-play manner. TPCORE has been developed as an IP core to execute fairly all the instruction set of the transputer while the inner architecture was different entirely. It can, therefore, run a program written in Occam, and make a network as the transputer since a TPCORE has also four os-link inerfaces. The clock frequency of TPCORE when it is implemented in an FPGA of Xilinx virtex4Lx160[5] is 24 MHz. If we form a TPCORE network with os-link in this chip, a mesh type connection with maximum 16 (4×4) TPCOREs can be implemented. The os-link is also operated in 24 MHz.

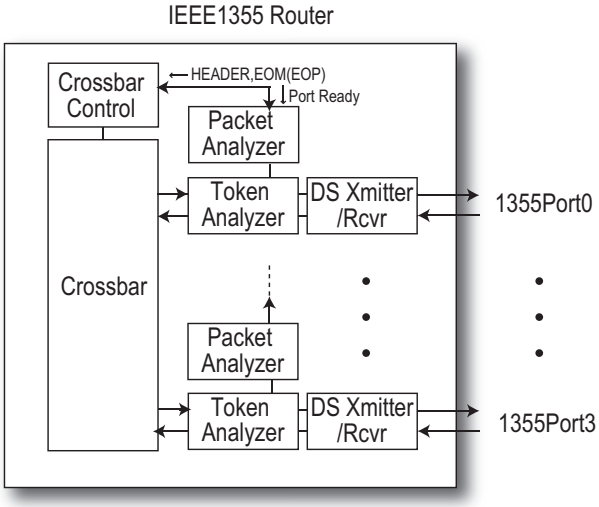

Figure 1: Block diagragm of presently developed IEEE1355 Router

2 IEEE1355 Network-Router with TPCOREs

Although the router currently developed has been based on IEEE1355 (hereafter this is also denoted as DS) standard, but SpaceWire, we expect that the router is adapted as a SpaceWire router with minor modification from similarity of these two standards. Block diagram of the router is shown in fig. 1. It is operated in 48 MHz, all the router operation is also synchronized with this clock. The number of DS ports is four, these ports are fully compliant with the DS protocol with bi-directional and high speed(48 M bit/sec.) transfer communication. Since a cascade link of a router to another one is possible, the network can be made further complex even if the number of the ports is only four. A non-blocking and wormhole crossbar switch enables a packet arriving at any port within two clocks

cently its complier which can be run under multi-thread environment of Linux has been developed[4].

[2]The os-link is a bit-serial protocol with unit of byte. For a byte transfer, sender sends it with 2-bit start- and 1-bit end-bit. Then receiver returns two bit acknowledge.

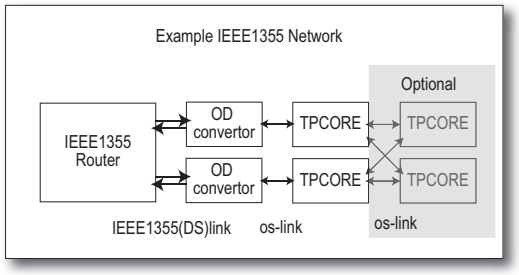

Figure 2: The example network setup with two (four) TPCOREs

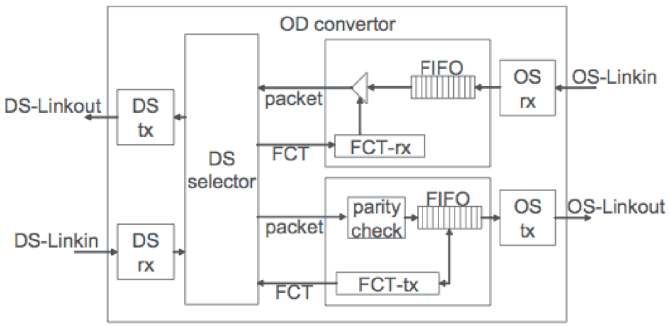

Figure 3: Block diagram of a bi-directional OD convertor (IEEE1355 $\leftrightharpoons$ os-link)

to relay over the other port of which the number is specified in the header part of the packet. Every DS port consists of DS transmitter/receiver, Token analyzer and Packet Analyzer. Token Analyzer picks up the parity bit, and checks it with parity actually observed in the previous token, it also transmits FCT (Flow Control Token) if there is a room to accept further tokens, or transmit tokens if FCT is received. Packet Analyzer picks up the destination port, which is written in the header part of a packet, and tells the Token Analyzer to start data transfer if the port is opened, and try to close the port when it receives EOP or EOM.

Figure 2 shows a network setup for the router functionality test. Since a TPCORE can communicate with each other using os-link, we have to implement an extra circuit to convert os-link to DS-link. The OD convertor does not only convert the data protocol to both direction (os $\leftrightharpoons$ DS-link) but also issue/receive FCT (Flow Control Token) signals. In fig. 4 an example of the signal sequence in OD convertor is demonstrated in which one byte data of 00111111_2 is formated into os-link, then converted to DS-link, and reverted to os-link. In fig. 5 the time sequence to transmit FCT is demonstrated. It is needed to send total 606 bits on DS-link for 32 byte data transfer. We measured this duration as 12.616μs while theoretical expectation is 12.625μs. The difference is less than the clock width(0.02μs).

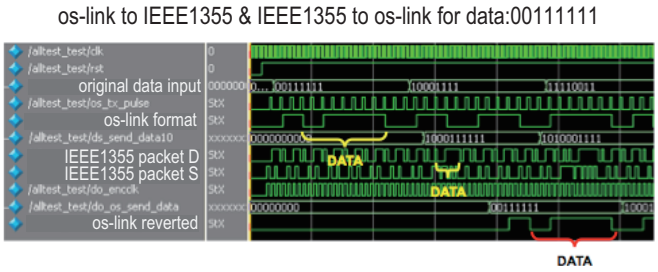

Figure 4: Time sequence of OD convertor. From a TPCORE, data:00111111_2 in os-link format is inputted, and converted to IEEE1355 protocol in an OD convertor, and this chart shows also data reverted to os-link format.

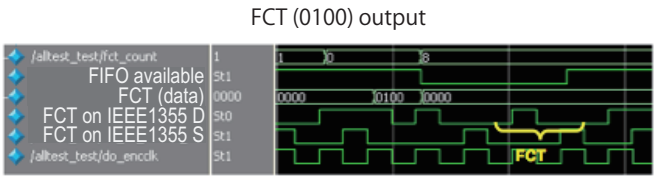

Figure 5: Timing chart to demonstrate the functionality of FCT transmission. If output FIFO for DS to os-link conversion part of an OD convertor has a room to accept data (FIFO available high), then FCT signal (bit sequence 0100_2 is transmitted over DS-link to prompt the data transmission side to send further eight tokens.

References

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[4] P.H.Welch and D.C.Wood, "The Kent Retargetable Occam Compiler", Proceedinga of Communication Process Architecture 1996 (CPA1996) held in Amsterdam, The Netherland, pp.143-166, IOS press.

[5] Xilinx, inc. Virtex 4: http://www.xilinx.com/products/virtex4/index.htm